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A METHOD OF FORMING A BORDERLESS CONTACT OPENING FEATURING A COMPOSITE TRI-LAYER ETCH STOP MATERIAL

BACKGROUND OF THE INVENTION

(1). Field of the Invention

The present invention relates to methods used to fabricate semiconductor devices, and more specifically to a method used to define a contact or via opening in a group of dielectric layers to expose an underlying conductive or isolation region of a semiconductor device.

(2) Description of Prior Art

Micro-miniaturization, or the ability to fabricate semiconductor devices with sub-micron features, has allowed improved device performance to be realized while still reducing the fabrication cost for the same semiconductor chips, comprised with the higher performing devices. Smaller features allow performance degrading parasitic capacitances to be reduced, while a greater number of smaller, higher performing semiconductor chips obtained from a specific size starting semiconductor substrate, result in a reduced fabrication cost for each specific semiconductor chip. The reduced area allotted to each semiconductor chip can however present difficulties not encountered for less dense semiconductor chips. For example contact or via openings formed in a group of dielectric layers, used to expose an underlying conductive

region and to subsequently accommodate a conductive via structure, can no longer afford the benefit of being fully landed on the underlying conductive region. The ability to form a non - fully landed contact or via opening, referred to as a borderless opening, is dependent on the ability of the etching procedure to completely remove dielectric material from all openings independent of the thickness uniformity of the dielectric layer across the entire semiconductor substrate. An over etch cycle used for the contact opening procedure, employed to insure complete removal of dielectric material independent of thickness uniformity, has to feature excellent selectivity to the exposed underlying materials so that the etch procedure terminates or significantly slows at end point. Unwanted removal of exposed conductive or insulator material during the over etch cycle can result in reduced device performance or yield loss.

This invention will describe a procedure for defining a contact or via opening in a stack of dielectric layers featuring a novel tri-layer composite located as the underlying material of the stack of dielectric layers. The etch rate selectivities of the components of the tri-layer composite allow a dielectric over etch cycle to be employed without risk of penetrating or removing the conductive or insulator regions needed to be exposed in the contact or via openings. Prior art such as Visokay et al, in U.S. Pat. No. 5,972,722, Hong, in U.S. Pat. No. 5,596,230, Parat et al, in U.S. Pat No. 5,731,242, and Wu et al, in U.S. Pat. No. 6,080,674, describe methods of forming self-aligned contact and via openings using underlying etch stop layers. None of these prior art however describe the unique tri-layer composite employed in the present invention, allowing the contact opening procedure to employ an over etch cycle without the risk of attacking or removing exposed underlying regions of the semiconductor device.

SUMMARY OF THE INVENTION

It is an object of this invention to define a contact or via opening in a stack of insulator layers to expose an underlying conductive region of a semiconductor device.

It is another object of this invention to employ a tri-layer insulator composite, located as an underlying component of the stack of insulator layers, to be used as a stop layer for the contact or via opening definition.

It is another object of this invention to employ a contact or via opening definition procedure featuring high etch rate selectivity between the overlying insulator layers and the underlying tri-layer insulator composite stop layer, to allow an extended insulator over etch cycle to be used to insure against thickness uniformity of the overlying insulator layer component of the stack of insulator layers.

In accordance with the present invention a method of defining a contact or via opening in a stack of insulator layers featuring an underlying tri-layer insulator composite, used as a stop layer during the dry etch contact opening definition procedure, is described. A tri-layer insulator composite comprised of an underlying silicon rich oxide layer, a hydro-silicon oxynitride (HOxSN) layer, and an overlying silicon nitride layer, is formed on the surface of a conductive or insulator region of an underlying semiconductor device. A boro-phosphosilicate glass (BPSG) layer and an overlying silicon oxide layer are next deposited on the tri-layer composite. After application of a bottom anti-reflective coating (BARC) layer, a photoresist shape is defined, and

used as an etch mask to allow an anisotropic reactive ion etch (RIE) procedure to define the desired contact or via opening in the silicon oxide and BPSG layers, with the dry etch procedure terminating in the silicon nitride component of the tri-layer composite. A critical over etch cycle is then employed to insure complete removal of insulator (BPSG and silicon oxide), accomplished a result of the high etch rate selectivity of silicon oxide to silicon nitride. Selective removal of silicon nitride via the anisotropic RIE procedure is followed by selective removal of the HOxSN component, with the dry etch procedure slowing at the appearance of the silicon rich oxide component of the tri-layer composite. Removal of the silicon rich oxide layer via a continuation of the anisotropic RIE procedure is selectively accomplished exposing a portion of the top surface of an conductive or insulator region of a semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiments with reference to the attached drawings that include:

Figs. 1 - 6, which schematically in cross-sectional style show key stages of a procedure used to define a contact or via opening in a stack of insulator layers, featuring an underlying tri-layer insulator composite used as a stop layer to allow an over etch cycle to be employed.

Figs. 7 - 8, which in cross-sectional style show a contact hole opening and via hole opening exposing underlying conductive regions of a semiconductor device, wherein the openings are defined in a stack of insulator layers featuring the underlying tri-layer composite.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of defining a contact or via opening in a stack of insulator layers featuring an underlying tri-layer insulator composite used as an etch stop layer, will now be described in detail. For description purposes Figs. 1 - 6, will show key stages used to define of an opening in a stack of insulator layers employing the novel underlying tri-layer etch stop component wherein the opening is shown exposing a top portion of a isolation region. However the same openings, contact or via openings, are shown in Fig. 7 - 8, exposing conductive regions of a semiconductor device. Semiconductor 1, comprised of single crystalline silicon, featuring a <100> crystallographic orientation, is used and schematically shown in Fig. 1. Isolation region 2, an element such as an insulator filled, shallow trench isolation (STI) region is formed in a top portion of semiconductor substrate 1. The STI region can be comprised of silicon oxide. If desired isolation region 2, can be a thermally grown, silicon dioxide field oxide (FOX) region. Formation of the tri-layer insulator composite, to be used as an etch stop during definition of a subsequent contact or via opening, is addressed. First silicon rich, silicon oxide layer 3, is formed to a thickness between about 100 to 200 Angstroms via plasma enhanced chemical vapor deposition (PECVD), via low pressure chemical vapor deposition (LPCVD), or via high density plasma chemical vapor deposition (HDPCVD) procedures. The deposition is performed using a ratio of silane or disilane, to oxygen or nitrous oxide, that results in a refractive index for silicon rich, silicon oxide layer 3, between about 1.485 to 1.55. The silicon rich feature of silicon oxide layer 3, will allow a desired etch rate selectivity to be realized during the definition of the contact or via opening. A liner layer comprised of HOxSN layer 4, is next formed via PECVD, LPCVD,

or HDPCVD procedures, at a thickness between about 200 to 500 Angstroms. Finally silicon nitride layer 5, to be used as the etch stop component of the tri-layer insulator composite during the definition and over etch cycles of overlying insulator layers, is deposited to a thickness between about 100 to 200 Angstroms via PECVD, LPCVD, or HDPCVD procedures. The result of formation of the tri-layer insulator composite, comprised of overlying silicon nitride layer 5, HOxSN layer 4, and underlying silicon rich, silicon oxide layer 3, are shown schematically in Fig. 1. The thicker overlying dielectric layers used for the bulk of insulation between conductive interconnect levels or between a conductive level and a conductive region in the semiconductor substrate, are next formed. Boro-phosphosilicate glass (BPSG) layer 6, is obtained at a thickness between about 1500 to 2500 Angstroms, via PECVD or LPCVD procedures. This is followed by formation of overlying silicon oxide layer 7, obtained at a thickness between about 5000 to 6000 Angstroms, again via PECVD or LPCVD procedures, using tetraethylorthsilicate (TEOS) as a source. This is also schematically shown in Fig. 1.

To reduce unwanted scatter during exposure of the photoresist layer to be used for the photoresist masking shape, bottom anti-reflective coating (BARC) layer 8, is applied at a thickness between about 500 to 700 Angstroms. BARC layer 8, can. be comprised of organic or inorganic material. A photoresist layer is next applied, exposed and developed, resulting in formation of photoresist masking shape 9, featuring opening 10a, comprised with a diameter between about 0.12 to 0.25 um. Opening 10a, exposes the top surface of the portion of insulator stack to be removed during the definition of the contact or via opening. The development cycle used to form opening 10a, in the photoresist layer may also extend through

BARC layer 8. This is schematically shown in Fig. 2.

Using photoresist shape 9, as an etch mask an anisotropic RIE procedure performed using CHF_3 as an etchant, is employed to define opening 10b, in silicon oxide layer 7, and in BPSG layer 6. The high etch rate ratio of silicon oxide or BPSG to silicon nitride, between about 5 to 1, to 10 to 1, allows this definition cycle to slow or terminate at the appearance of the top surface of silicon nitride layer 5. This is schematically shown in Fig. 3.

The procedures used deposit silicon oxide layer 7, and BPSG layer 6, can result in unwanted thickness uniformity across the semiconductor substrate. Therefore to account for possible thickness distributions of insulator layer, an over etch cycle is employed as a critical component of the contact or via opening definition procedure. The presence of silicon nitride layer 5, with a lower etch rate than silicon oxide or BPSG in CHF_3, allows an over etch cycle to be included as a component of the anisotropic RIE procedure. The over etch cycle is performed for a time between about 30 to 60 sec., allowing excess silicon oxide or BPSG to be possibly removed, while only between about 50 to 150 Angstroms of silicon nitride layer 5, is removed. Opening 10c, experiencing the over etch cycle, is now schematically shown in Fig. 4.

Selective removal of the tri-layer insulator composite is next addressed and schematically described using Figs. 5 - 6. The anisotropic RIE procedure used to define the desired opening in silicon oxide layer 7, and in BPSG layer 6, and used to supply the desired over etch cycle, is now continued using CF_4 or Cl_2 as a selective etchant for silicon nitride layer 5, and for HOxSN layer 4, resulting in opening 10d, schematically shown in Fig. 5. The higher etch rate of silicon

nitride and HOxSN layer 4, in CF_4, when compared to silicon rich, silicon oxide layer 3, allows this cycle to terminate in silicon rich, silicon oxide layer 3. The anisotropic RIE procedure is now continued, again using CHF_3 as an etchant, allowing exposed portions of silicon rich, silicon oxide layer 3, to be removed resulting in opening 10e, exposing a portion of the top surface of STI region 2. The use of the tri-layer insulator composite, featuring stop layer properties, allowed the needed over etch cycle to be employed without risk of etching or penetrating into the underlying material, STI region 2, in this case. Photoresist shape 9, as well as BARC layer 8, are now removed via plasma oxygen ashing procedures. This is schematically shown in Fig. 6.

The process illustrated in Figs. 1 - 6, featured a generic description of a procedure used to define a contact or via opening in a stack of insulator layers comprised with an underlying tri-layer insulator composite used as a stop layer for the dry etch definition procedure. Fig. 7, schematically shows an example of this invention in which borderless contact opening 10f, is formed with the above dry etch definition procedure. The stop layer properties of the tri-layer insulator composite allowed the selective anisotropic RIE procedure to expose a portion of a top surface of conductive region 11, without gouging or penetration at the surface of the conductive region. Conductive region 11, can be a source/drain region, or a metal silicide layer formed on an underlying area such as a source/drain region. Another example of the use of the tri-layer insulator composite as a component of an insulator stack is shown schematically in Fig. 8, wherein via opening 10g, is defined using an anisotropic RIE procedure. The presence of the tri-layer insulator composite, comprised of silicon nitride layer 5, HOxSN layer 4, and silicon rich, silicon oxide layer 3, allowed the dry etch procedure to successfully define via opening 10g,

while terminating at the appearance of a portion of a top surface of conductive region 12, wherein conductive region 12, can be a metal interconnect structure.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is: